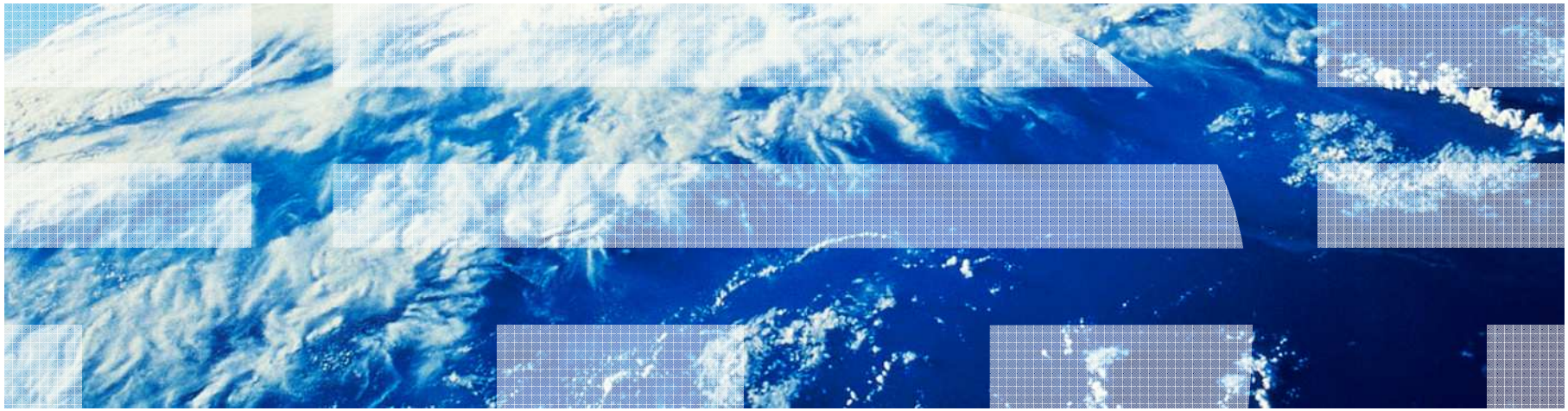
EUVL Symposium, Miami, Florida
October 17, 2011

EUV masks: ready or not?

Emily Gallagher[a], Karen Badger[a], Louis Kindt[a], Mark Lawliss[a], Gregory McIntyre[b], Alfred Wagner[c] John Whang[a]

[a] IBM Microelectronics, 1000 River St., Essex Junction, VT 05452
[b] IBM Microelectronics, 257 Fuller Road, Albany, NY 12203
[c] IBM Research, 1101 Kitchawan Road, Yorktown Heights, NY 10598



Outline

- EUV mask readiness is a huge topic
  - Many companies heavily engaged internally
  - Recently the subject of a plenary session at SPIE Photomask 2011
    "Is it too late to panic? EUV is Real!"
- This presentation
  - Is NOT a review of ITRS roadmaps
  - Is NOT a summary of all technical material presented in the last year (though some references are included)
  - IS a balanced assessment of mask readiness for pilot line work in 2013

Introduction

*"A **rubric** is an assessment tool for communicating expectations of quality." - Wikipedia*

- To answer the readiness question, review mask readiness in six key areas:
  - Mask processing
  - Blank
  - Mask defectivity (as built)
  - Mask defectivity (as used)
  - OPC
  - Black border

- Included development areas that are not purely "mask" because of tight linkage to successful EUV solution

EUV rubric	2013 pilot *outlook*
Mask process	
Mask blank	
Mask defectivity (as built)	
Mask defectivity (as used)	
OPC	
Black border effect	

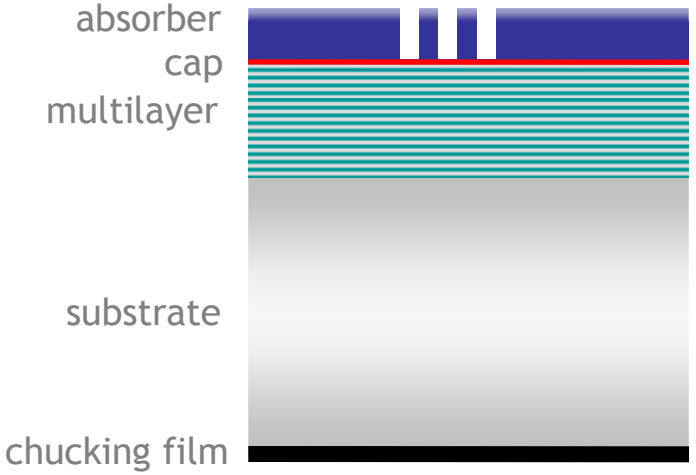
likely with work
possible with significant work
possible with significant work, investment & time

E. Gallagher et al. "EUV masks: Ready or not?"

Mask process: general results

- EUV mask process achieves CD control comparable to optical masks
  - Sample data from clear feature on positive resist mask in table
  - Already meet 2012 targets for CD & IP

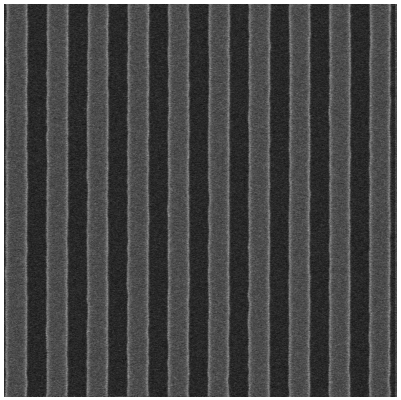
EUV mask schematic



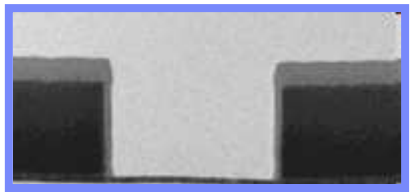
EUV test mask data **(nm@4X)**	2011	2012 ITRS tgt*
CD uniformity (3σ) 100nm clear	1.6	3.3
Linearity 60-1000nm clear	4.9	5.4
Image placement (3σ)	4.0	4.8

** ITRS, 2010*

SEM image



SEM cross section



E. Gallagher et al. "EUV masks: Ready or not?"

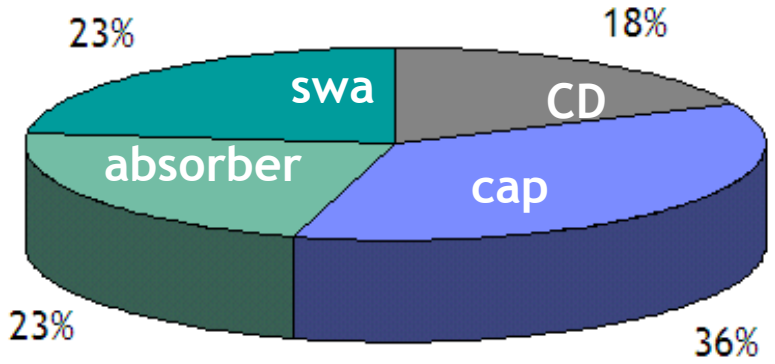
Mask process: CD

- Two reasons for EUV-specific development to meet targets across all densities:

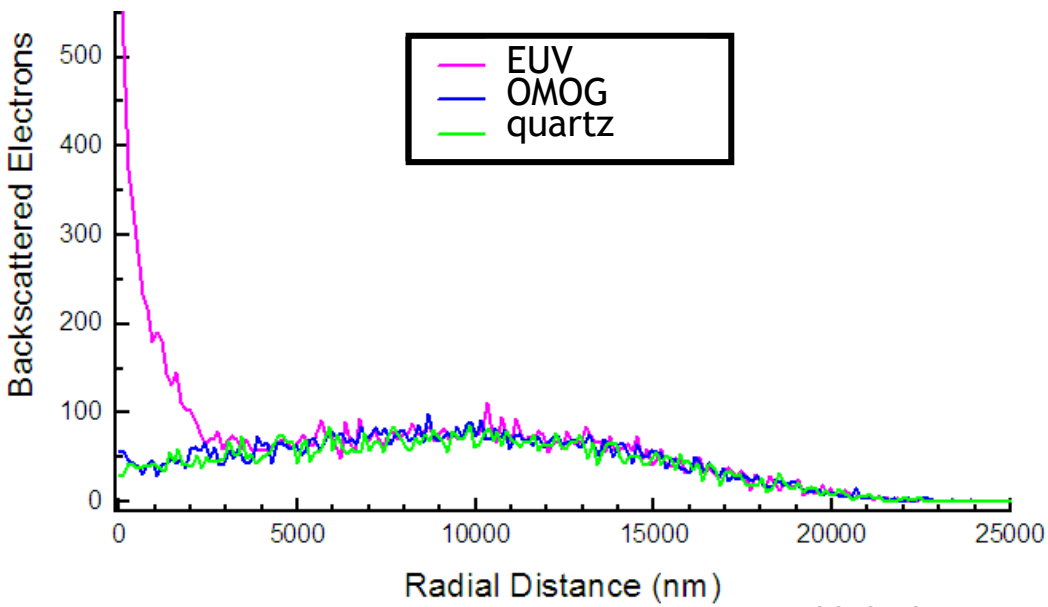
1. Mask CD variations are not the only contributor to wafer CD variations

2. Electron backscattering of EUV mask films differs from binary optical films (OMOG), changing ebeam proximity correction requirements
   - Modified PEC kernel
   - Smaller correction grid

mask impact on wafer CD



Gallagher et al., IBM, SPIE 7969-30 (2011)

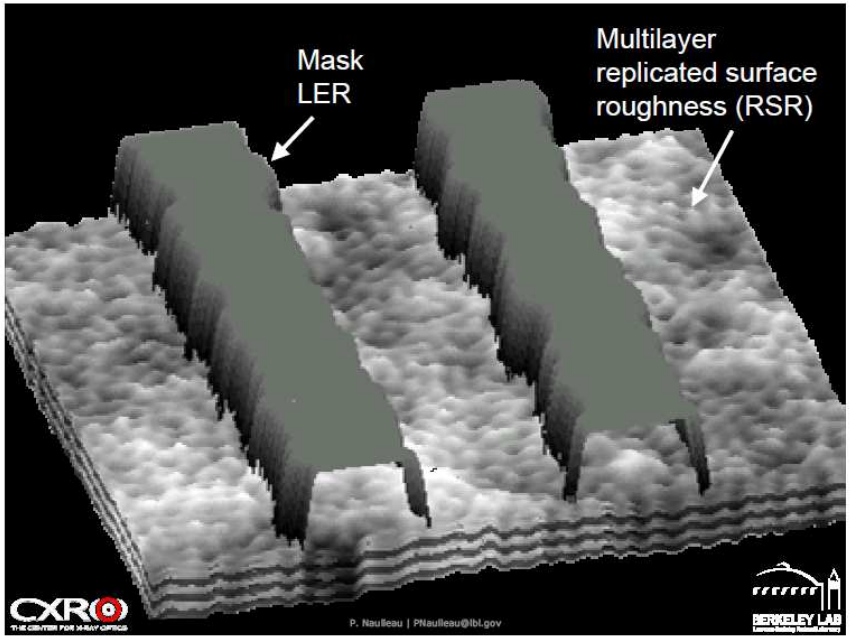


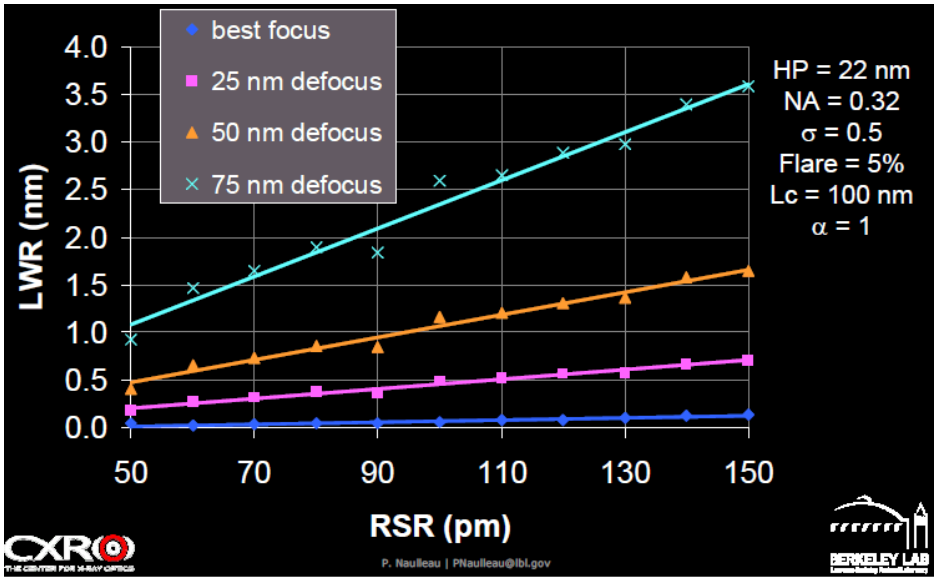
A. Wagner, unpublished, 2011

E. Gallagher et al. "EUV masks: Ready or not?"

Mask process: roughness

- Three components to roughness:
  1. Line Edge Roughness (LER)
     - Mask component of wafer LWR is ~2nm (4X) for 2012
     - Current mask processes LER 3-4nm
  2. Replicated surface roughness (RSR)
     - AFM tends to over-predict RSR
     - Primarily increases LWR at defocused exposure (adds in quadrature)
  3. Capping layer roughness
     - Lower order effect
- Process development needed, but not likely to gate pilot development





Patrick Naulleau, CXRO at LBL, SPIE 8166-04 (2011)

E. Gallagher et al. "EUV masks: Ready or not?"

Mask process summary

Readiness for 2013 pilot:

- Possible with significant work on minimizing roughness and improving ebeam corrections

EUV rubric	2013 pilot *outlook*
Mask process	

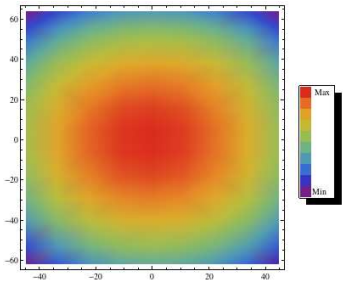
E. Gallagher et al. “EUV masks: Ready or not?”

Mask blank: non-flatness

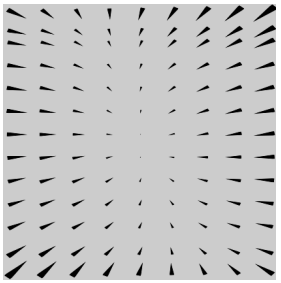
- Wafer image placement errors are generated by non-flat EUV masks
  - In plane distortion (IPD)
  - Out of plane distortion (OPD)

- Masks will not be perfectly flat, despite progress; development needs:
  - Determine flatness requirement because tradeoffs exist with substrate defectivity
  - Develop compensation during ebeam write, predicated on repeatable chucking

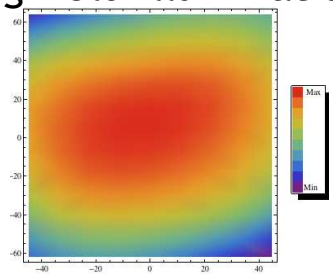
non-flatness + surface distortion from chucking



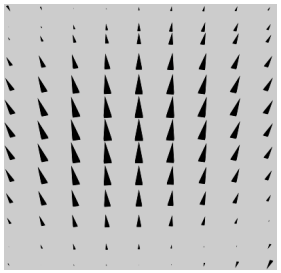
wafer IPD



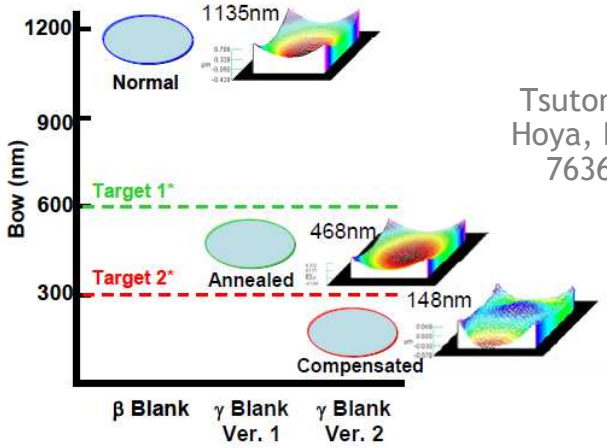
thickness variation + ring field illumination



wafer OPD



Sudhar Raghunathan, unplublished, 2009



Tsutomo Shoki, Hoya, Proc. SPIE 7636 (2010)

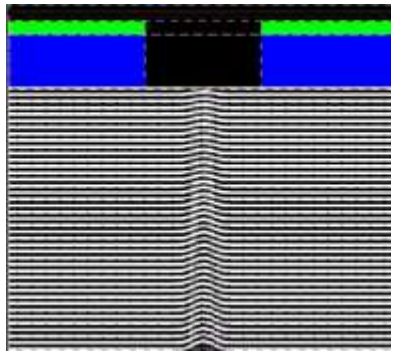
* Based on SEMI P37 standard

E. Gallagher et al. "EUV masks: Ready or not?"

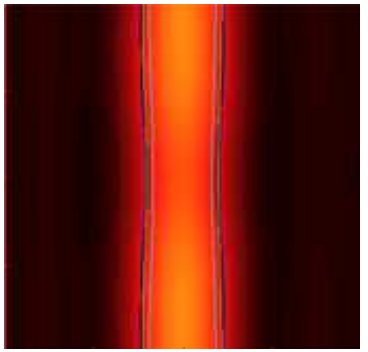
Mask blank: defects

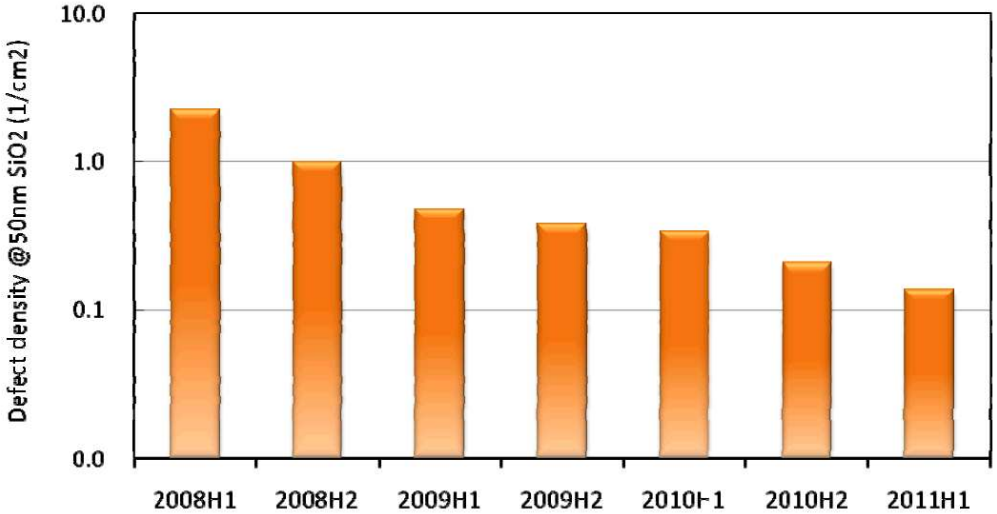
- Multilayer defects become printable phase defects on masks
- Blank defect trends are improving
  - Example of AGC data shown
  - Assuming maximum printable field size, #defects of concern:
    - ~ 15 ML defects 1H11
    - ~ 10 ML defects 1H13
- Mask blanks will have some defects
  - *Mitigation methods will be needed*

Simulation of ML defect



top down: impact on clear line





Yusuke Hirabayashi, AGC, SPIE 8166-140 (2011)

E. Gallagher et al. "EUV masks: Ready or not?"

Mask blank summary

Readiness for 2013 pilot:

- Suppliers are making progress on both defect levels and flatness but both need mitigation efforts in the mask house
- For more detail… Session 8 “Critical assessment of substrate and mask blank readiness” Ted Liang

EUV rubric	2013 pilot *outlook*
Mask process	
Mask blank	

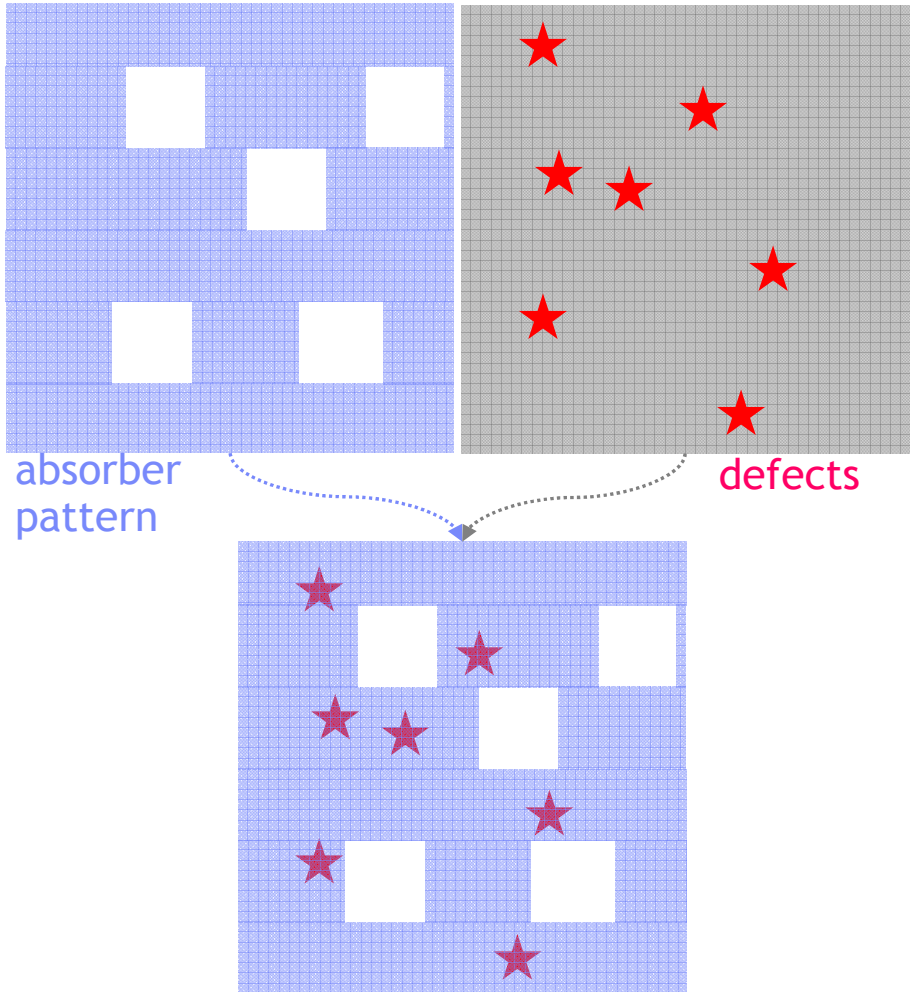
E. Gallagher et al. “EUV masks: Ready or not?”

Defect avoidance by pattern shift

- Illustration of concept
  - Blank with 7 defects
  - Contact mask design
  - Position design relative to blank defects so that all defects fall under absorber

Analysis on IBM designs to answer:

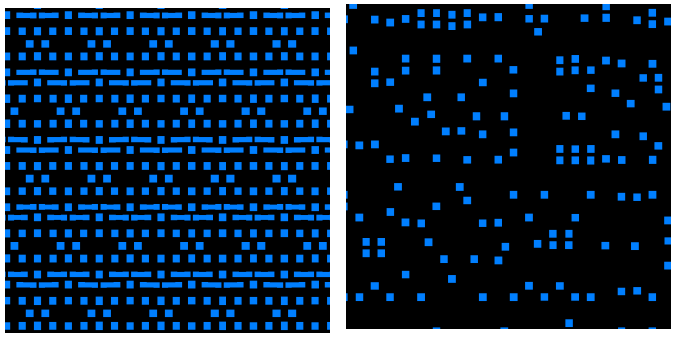
1. What fraction of defects intercept mask features?
   - With and without pattern shifts
2. Probability of eliminating all blank defects using pattern shift
   - Number, size and shape of defects
   - Contact, metal and via levels
   - Shift field size

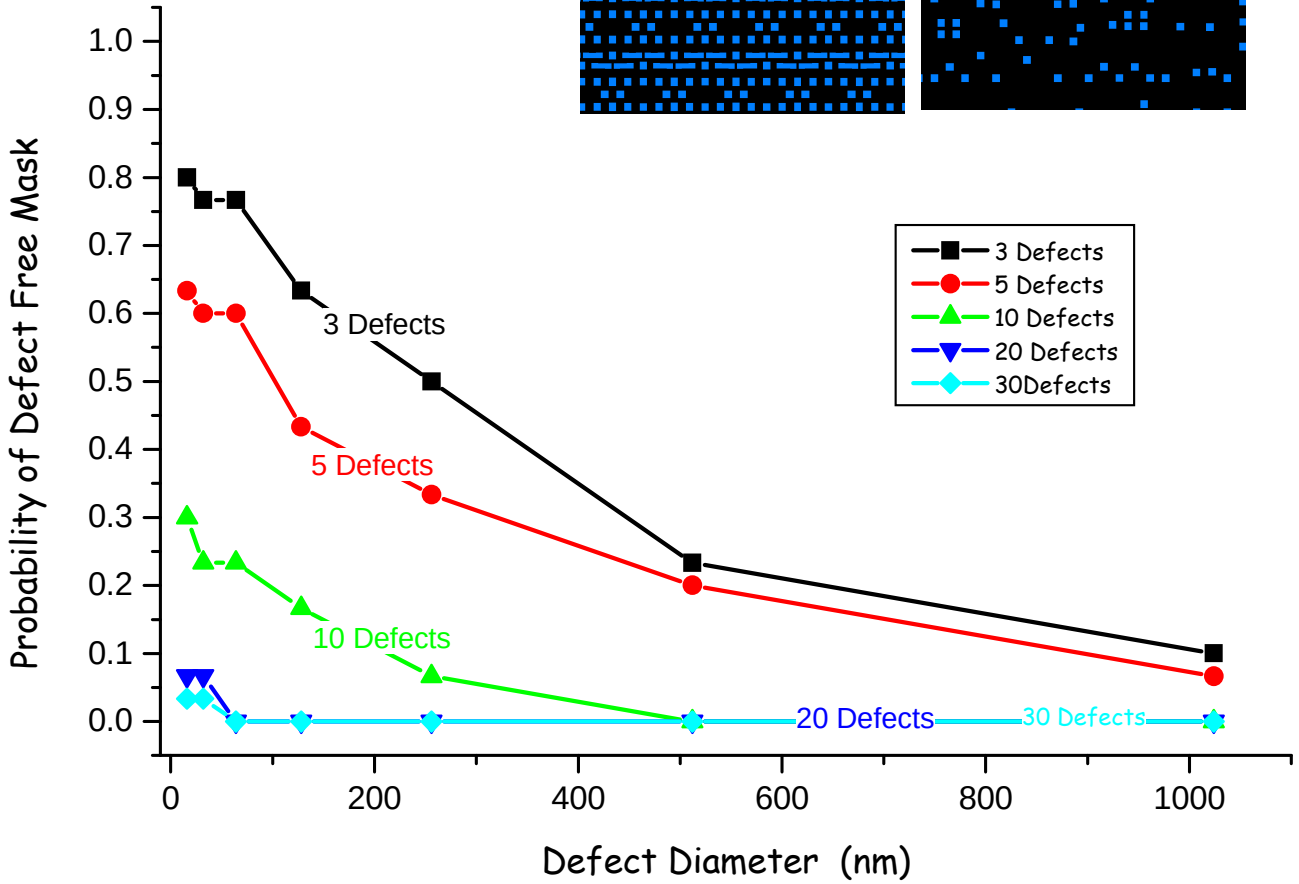


E. Gallagher et al. "EUV masks: Ready or not?"

Defect avoidance: motivation

- Explore probability of building a defect free mask as a function of defect size
- Contact design data with 8.3% open area
- No pattern shift applied
- *Without pattern shift, very low probability of building a defect free mask*



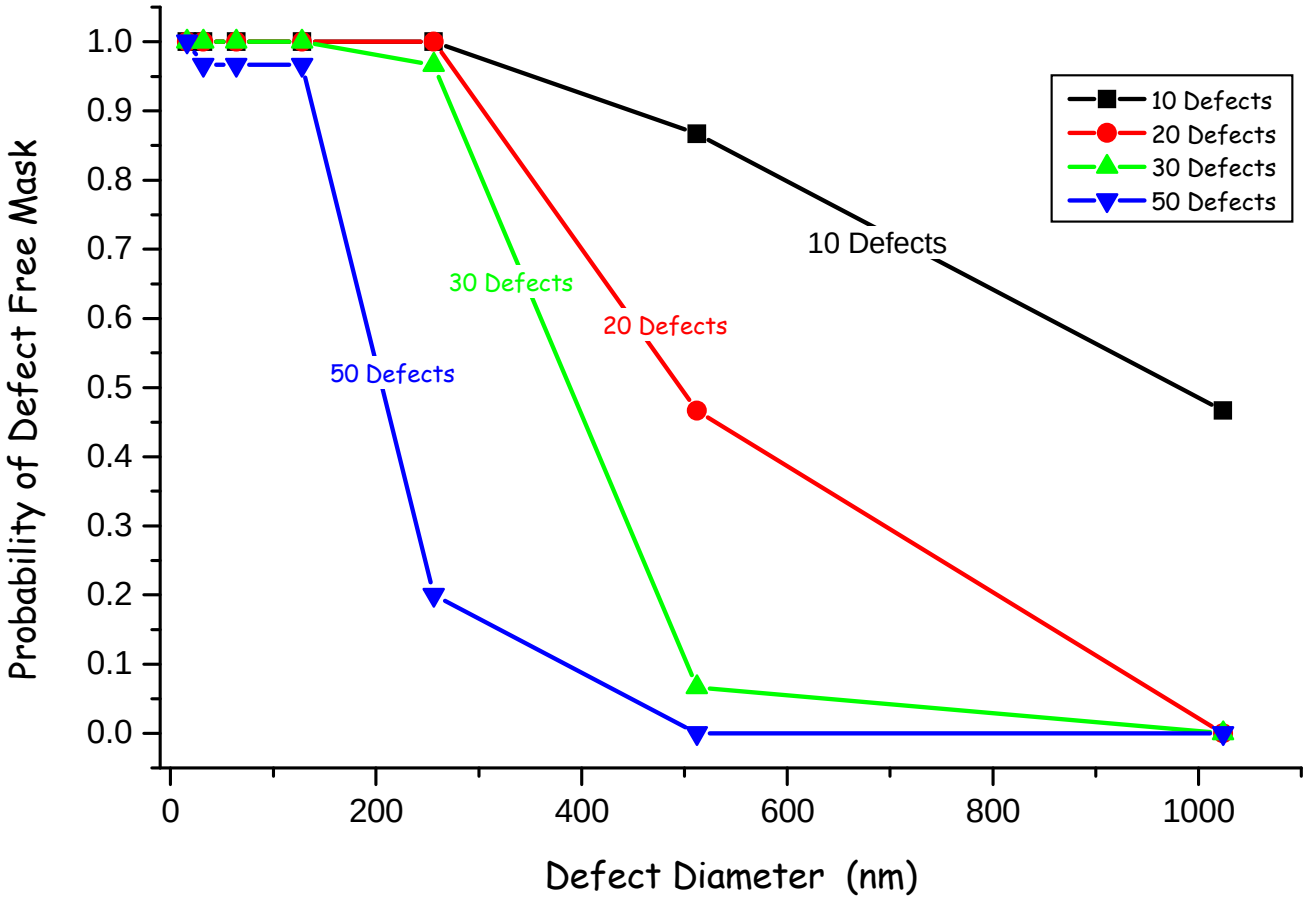


A. Wagner, unpublished, 2011

E. Gallagher et al. "EUV masks: Ready or not?"

Defect avoidance: pattern shift

- Explore the effect of blank defects on mask yield with pattern shift on the same contact design data
  - Up to 16um pattern shift in x or y
- *Large defects will impact yield*
- *~30 defects is the upper limit for reasonable yield*
- Feasible!



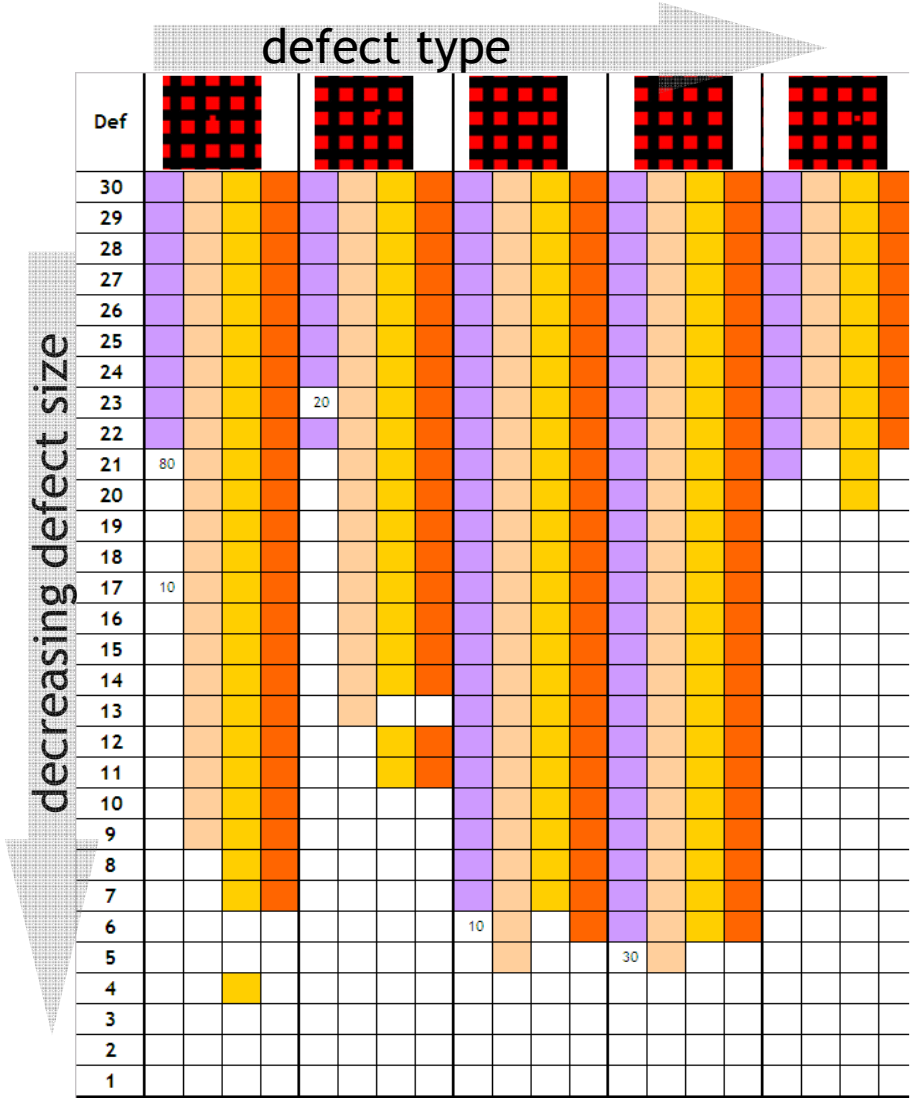
A. Wagner, unpublished, 2011

E. Gallagher et al. "EUV masks: Ready or not?"

Patterned inspection

- Inspection capability can be verified using standard methods:
  1. Build programmed defect masks
  2. Inspect on multiple tools
  3. Determine detect threshold
  4. Establish whether defect sensitivity is sufficient

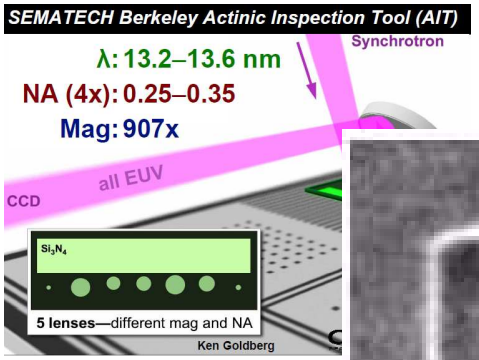
- Example here includes optical and ebeam patterned inspection
- *Printability of defects must be included in assessment*

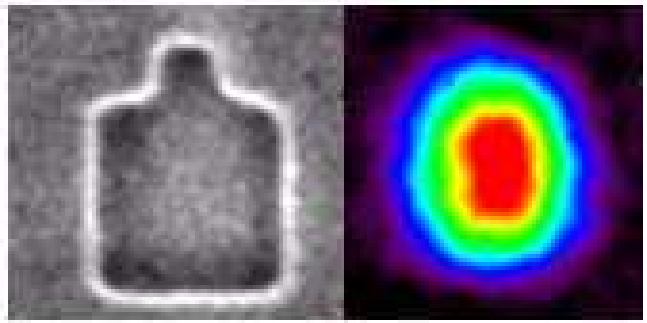


E. Gallagher et al. "EUV masks: Ready or not?"

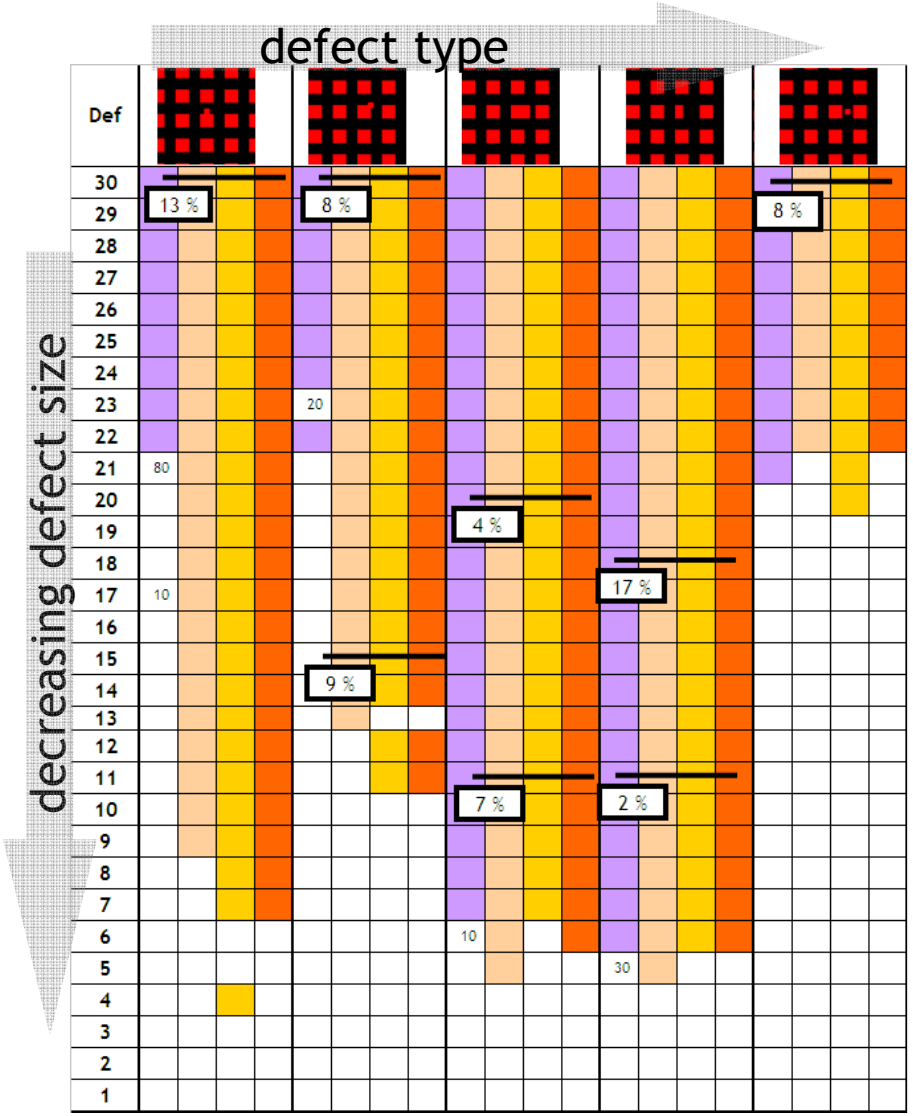
Defect verification

- Commercial actinic tools are not yet available
- Options for pilot production include
  - Wafer print
  - Actinic Inspection Microscope (AIT)
  - Other research tools
- AIT used on selected defects to determine printability





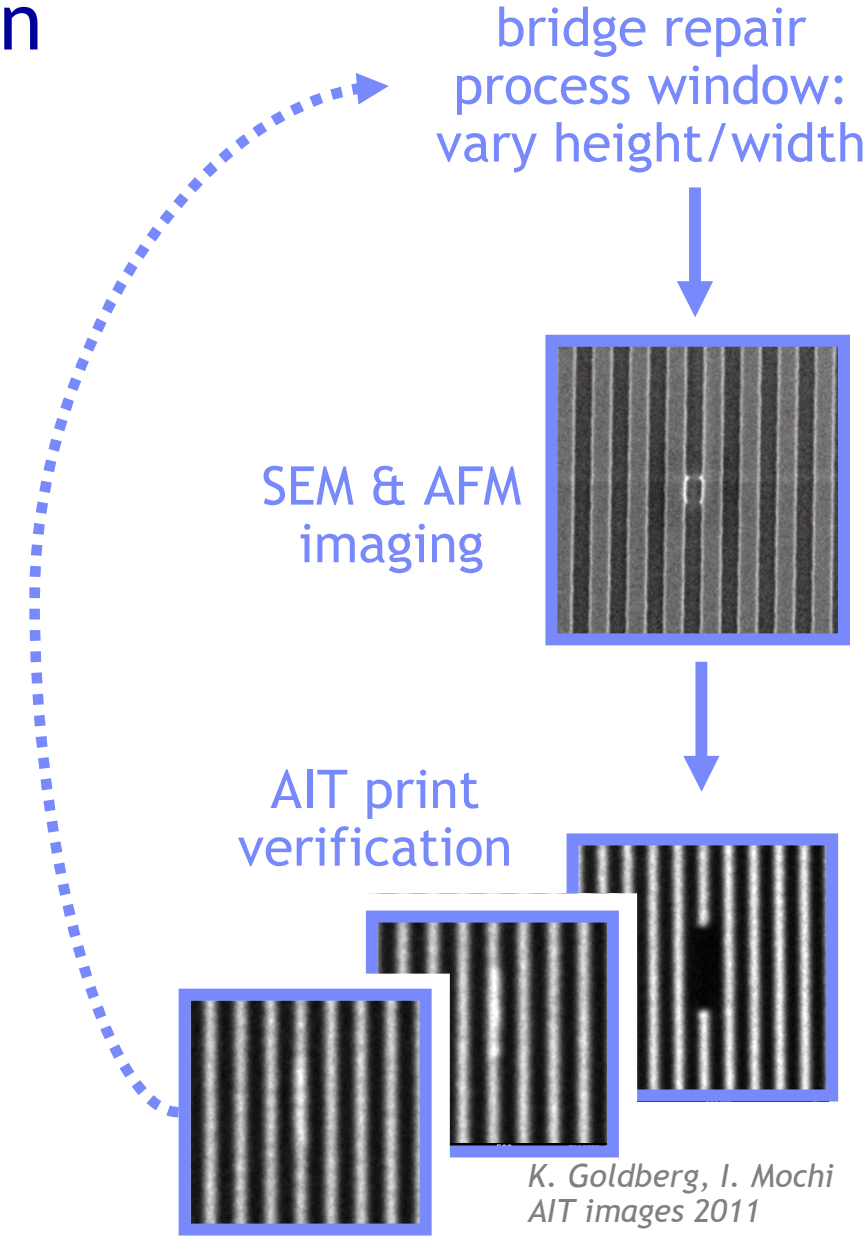
K. Goldberg I. Mochi, AIT images 2011



E. Gallagher et al. "EUV masks: Ready or not?"

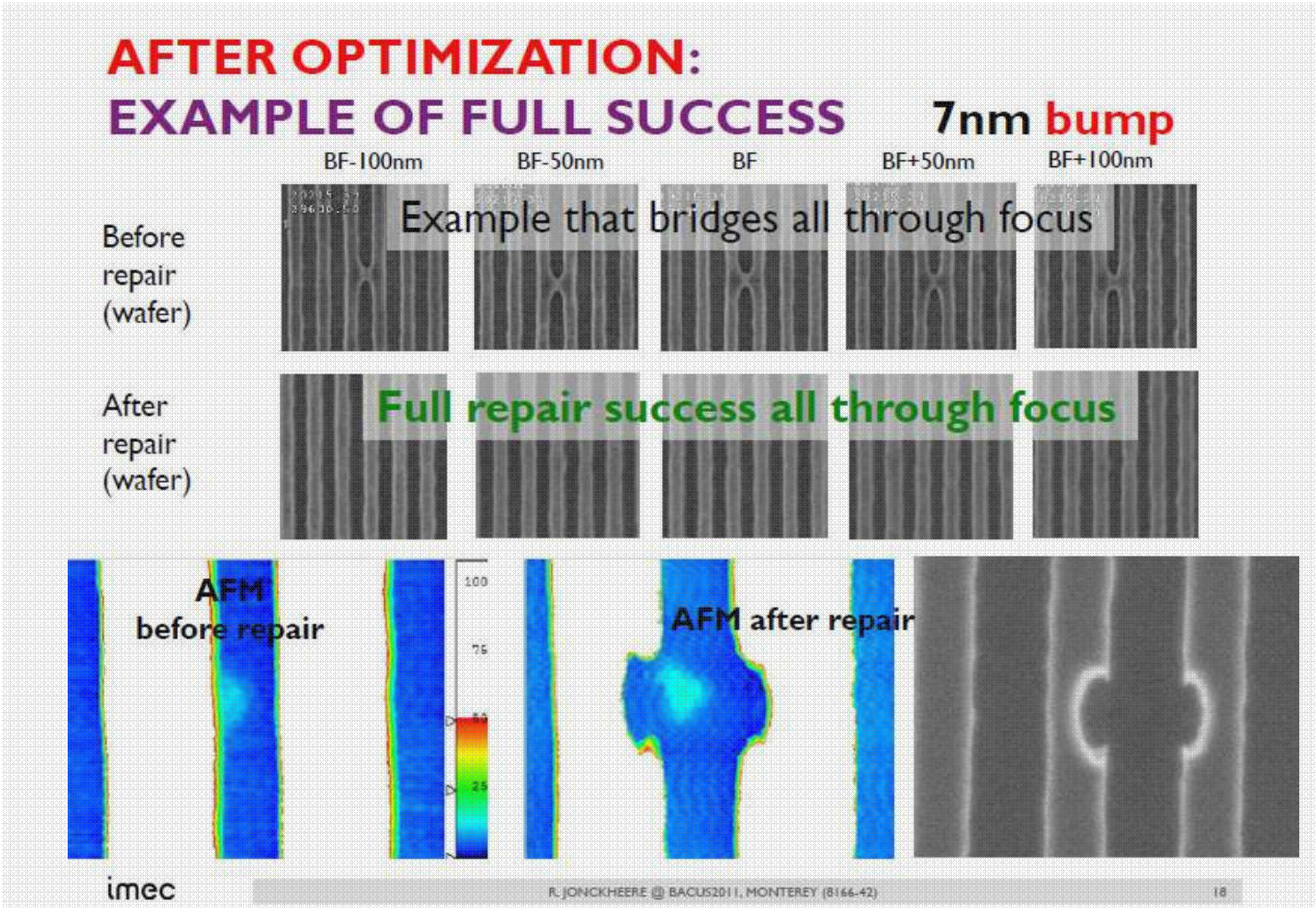
Defect repair & verification

- Example illustrates sample bridge repairs that were not optimized and would require process modifications
- *Repair process learning demands feedback on printability*
  - *SEMs, AFMs and non-actinic inspection are not sufficient*
  - *Feedback is slowed by AIT and/or wafer verification*



E. Gallagher et al. "EUV masks: Ready or not?"

Defect repair & verification



R. Jonkheere, IMEC, SPIE 8166-42 (2011)
& in Session 9: "Progress towards defect-free EUV reticles for NXE3100"

E. Gallagher et al. "EUV masks: Ready or not?"

Mask defectivity (as built) summary

Readiness for 2013 pilot:

- Feasible but…
- Successful pattern shift requires:
  - Excellent coordinate accuracy
  - Low-defect fiducial process
  - Infrastructure for sorting blanks and patterns
- All printing defects need to be detectable
- Repairs remain challenging

EUV rubric	2013 pilot *outlook*
Mask process	
Mask blank	
Mask defectivity (as built)	

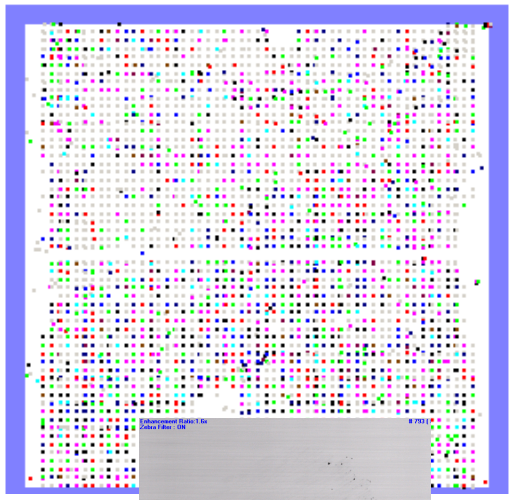
E. Gallagher et al. "EUV masks: Ready or not?"

Mask defectivity: handling & defects

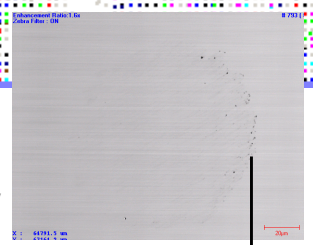
- No EUV pellicle exists today
- Dual pod solution alternative
  - E152 EUV pod standard established in 2009 but still in flux
  - Absence of single pod for mask finish to wafer exposure (including shipping)
- Areas of concern for defect and contamination:
  - Electrostatic chuck contact
  - Shipping
  - Handling
  - Storage
- *Cleaning will improve mask lifetime, but not solve all issues*

Example of e-chucking accelerated damage on ADT

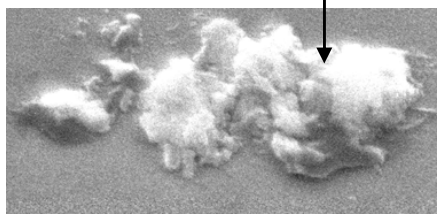
inspection post 6X chucking



Microscope view of defect



SEM of particle

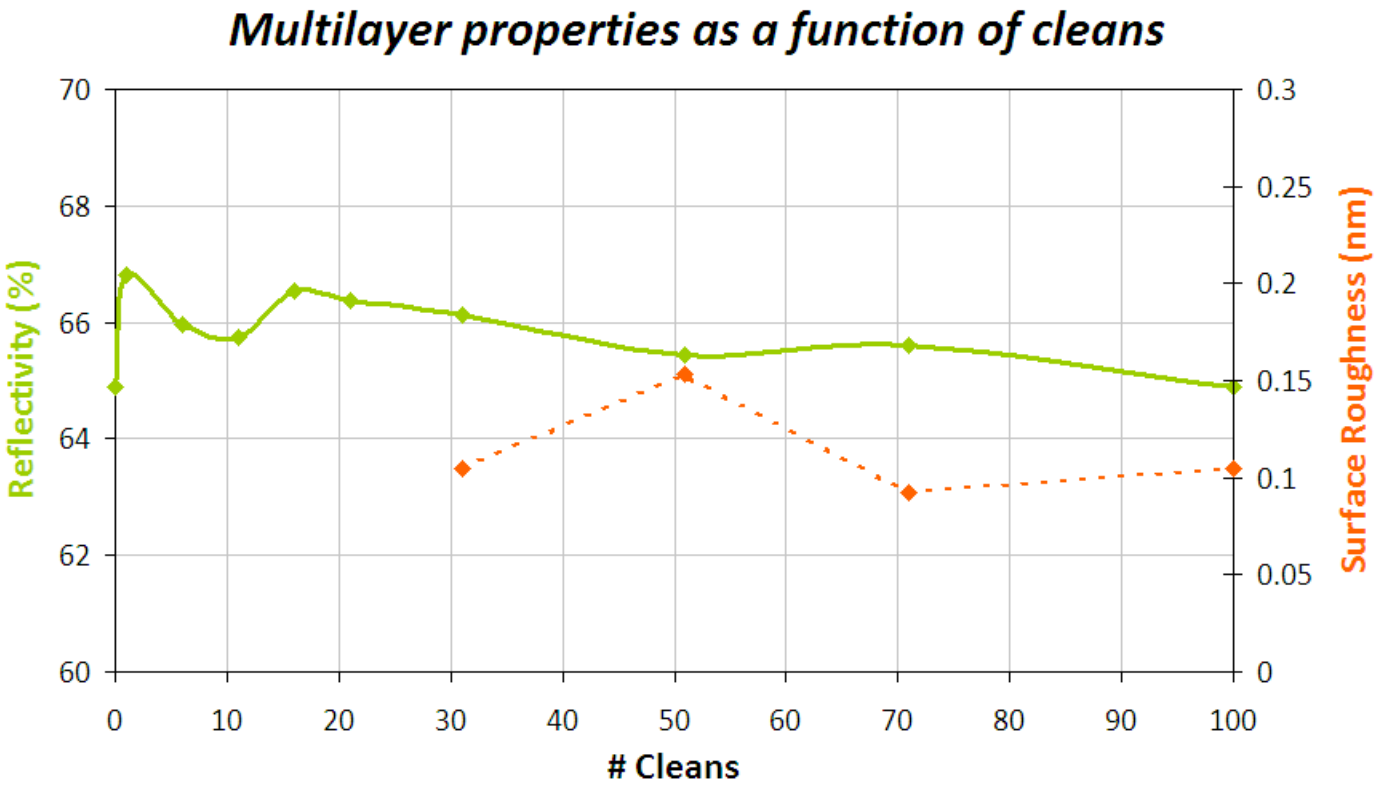


O. Wood, EUVL Litho Symposium, 2010

E. Gallagher et al. "EUV masks: Ready or not?"

Mask defectivity: cleaning durability

- Excellent cleaning durability obtained
- >99% removal efficiency
- After 100 cleans Ru cap integrity confirmed with TOFSIM
- No one can yet test full fluence effects of mask materials



E. Gallagher et al. "EUV masks: Ready or not?"

Mask defectivity (as used) summary

Readiness for 2013 pilot:

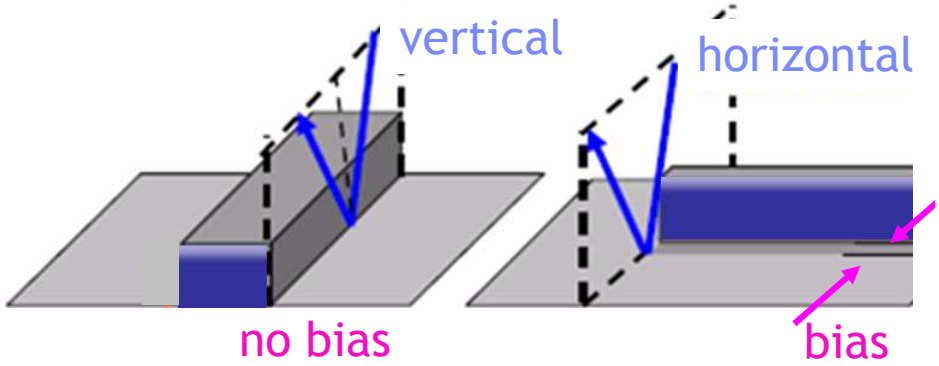
- Yields are likely be plagued by particle adders and contamination

EUV rubric	2013 pilot *outlook*
Mask process	
Mask blank	
Mask defectivity (as built)	
Mask defectivity (as used)	

E. Gallagher et al. "EUV masks: Ready or not?"

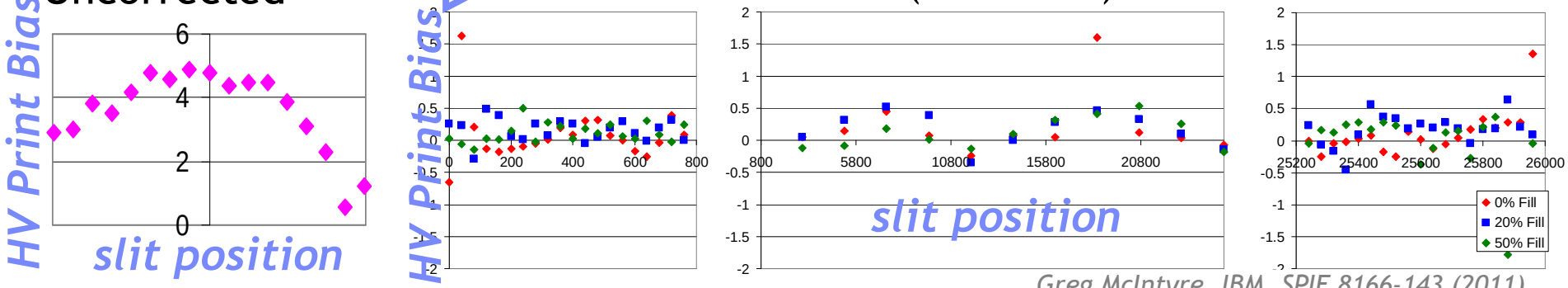
OPC: Shadow effect

- 3D feature & exposure angle creates orientation-dependent shadow
- Simple 1D horizontal-vertical (HV) bias appears sufficient for simple patterns
- Smaller and complex patterns will probably need 2D models



Shadow correction: 70nm thick absorber

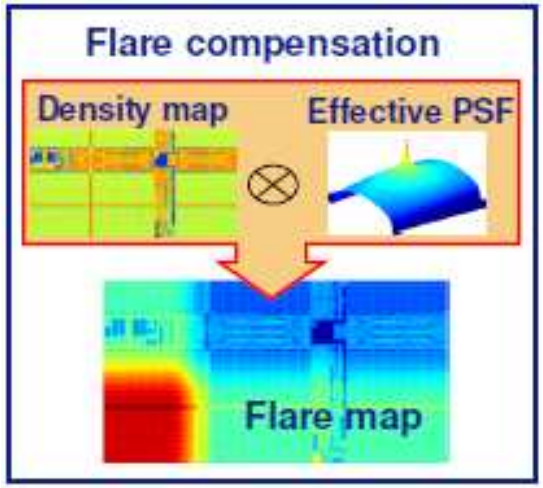
Uncorrected → HV bias correction (2nm max)



Greg McIntyre, IBM, SPIE 8166-143 (2011)

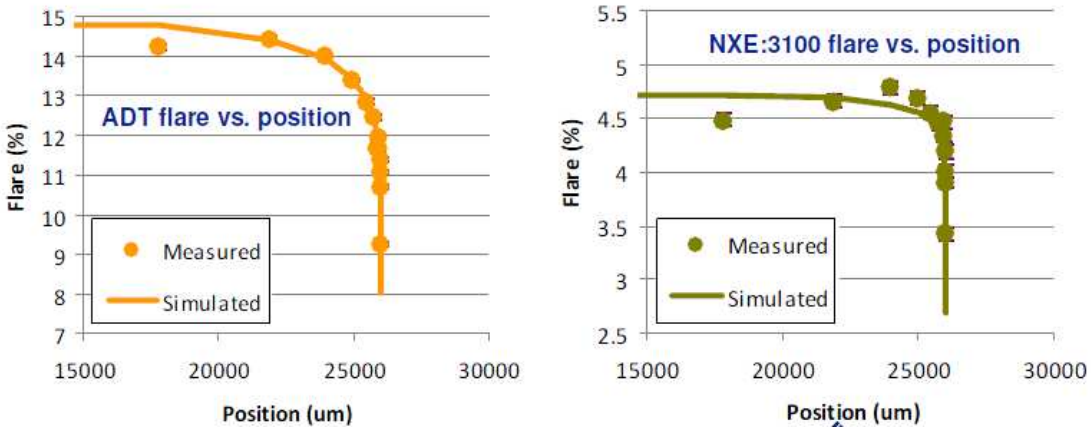
E. Gallagher et al. "EUV masks: Ready or not?"

OPC: flare



- Flare ~ unwanted light that reaches the wafer resist
  - Includes scatter from optics and mask
  - Nominal flare map calculated assuming ideal binary mask
- Non-correctable flare is the concern
- Increased reflectivity (thinner absorber) adds intensity to dark regions
- May need to include finite EUV absorber reflectivity (1-2%)

Through slit flare	ADT	NXE:3100
Maximum	<15%	< 5%
Range	~ 7%	~ 2%



Frank Driessen, ASML, SPIE 8166-23 (2011)

E. Gallagher et al. "EUV masks: Ready or not?"

OPC (mask-specific) summary

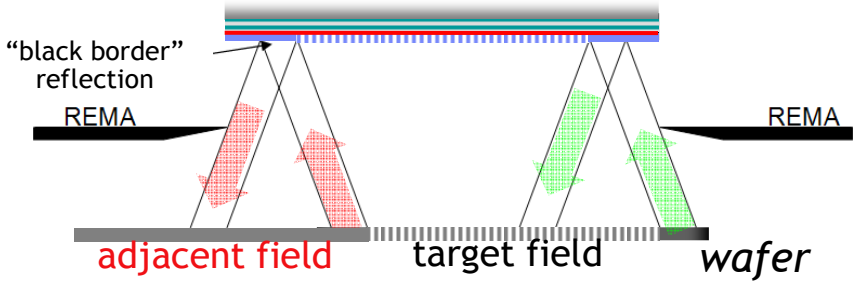
Readiness for 2013 pilot:

- EUV OPC methods build on optical ones, but rely on stability of the mask and lithography
- For more detail… Session 5 "*Shadowing effect compensation requirements for 15nm node EUV lithography" S. Raghunathan, O.Wood*

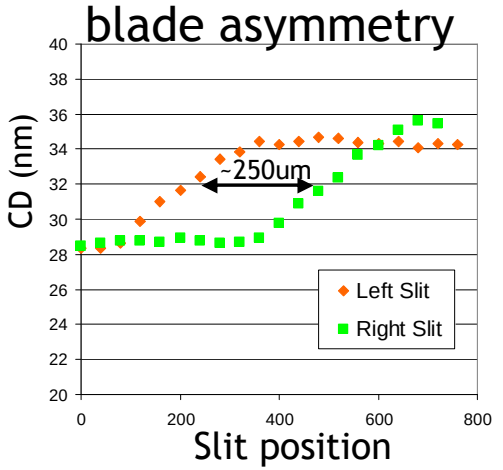
EUV rubric	2013 pilot *outlook*
Mask process	
Mask blank	
Mask defectivity (as built)	
Mask defectivity (as used)	
OPC	

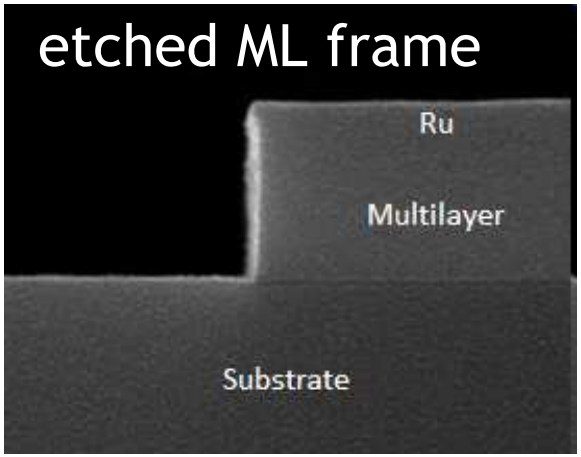
E. Gallagher et al. "EUV masks: Ready or not?"

Black border



- Two solutions for source light that is not blocked by the ReMa blade
- OPC correction
  - Effectiveness of OPC compensation depends on stability of blade position
    - Recent ADT data shows left-to-right asymmetry
    - NXE3300 ReMa may support OPC solution
  - Requires edge die exposures to ensure the full fields have the same OPC compensation (throughput concern)
- Frame or "black border" on mask
  - Process developed and demonstrated*
  - Impact to defectivity and lifetime must be quantified





** For example, Takashi Komo, Selete J. Micro/Nanolith. MEMS MOEMS 9, 023005 (2010)*

E. Gallagher et al. "EUV masks: Ready or not?"

Conclusion

- All mask areas require development
- Defectivity remains the largest concern and will impact yield for pilot production in 2013
- Lack of actinic tools demands wafer print and leveraging actinic metrology tools for process & defect verification

EUV rubric	2013 pilot *outlook*
Mask process	
Mask blank	
Mask defectivity (as built)	
Mask defectivity (as used)	
OPC	
Black border effect	

likely with work
possible with significant work
possible with significant work, investment & time

E. Gallagher et al. "EUV masks: Ready or not?"

EUV masks: ready or not?

EUV masks could be ready

for 2013 pilot…

but only with increased focus and investment

E. Gallagher et al. “EUV masks: Ready or not?”

Acknowledgements

- IBM's mask house engineering and manufacturing teams for mask builds and processing
- Sematech for Mask Blank Development Center metrology and AIT time
- Rik Jonkeere (IMEC), Patrick Naulleau (CXRO), Kenneth Goldberg (CXRO), Iacopo Mochi (CXRO), Obert Wood (GLOBALFOUNDRIES), Sudhar Raghunathan (GLOBALFOUNDRIES)

Note: Portions of this work were performed by the Research Alliance Teams at various IBM Research and Development Facilities.

THANK YOU